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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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IP ADMINISTRATION
LEGAL DEPARTMENT 20BN
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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/444,173	PONG, FONG	
	Examiner	Art Unit	
	Jasmine Song	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The rejection of claims 1-20 is **maintained**.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al., U.S. Patent 6119204.

Regarding claims 1,9 and 19, Chang et al. teach a method for accessing memory in a multiprocessor system, the method comprising:

from a requesting processor, issuing a request for a block of data to one or more other processors and memory is taught as interconnect 16 includes a broadcast fabric , each device connected to interconnect 16 preferably snoops all communication

transactions on interconnect 16 (Fig.1, 2 and 3, col. 7, lines 35-38 and col.4, lines 23-34), each copy of the block of data being associated with state information indicating whether the copy is valid or invalid is taught as sourcing data cached within cache hierarchy 36 on interconnect 16, updating the coherency state of cached data, invalidating entries within the TLB of processor 10 (Fig.2, col.4, lines 47-62);

in each of the processors and memory that receive the request, checking to determine whether a valid copy of the block of data exists (col.7, lines 39-43); and

returning a valid copy of the requested data from one of the other processors or memory is taught as a snooping processor provides an appropriate response to initiating processor (col.11, lines 46-52).

Chang does not specifically teach that only one processor or memory responds to the request for the valid data. However, it is well known in the memory art of multiprocessor systems for the ownership of the requested data be a necessary component in which element provides the valid data to the requesting device. In order to maintain coherency of data within these systems only one processor will have the ownership rights for changing the data and depending on other activities in the system, the data may be in a modified state and either written back to the main/shared memory or held by that processor in a memory (cache, buffer or other type memory) until it is time to perform the write-back operation to update the main/shared memory. In this situation, the valid data can only be provided by the processor that owned the data in a state that allowed the data to be modified or by the main/shared memory if the modified data has been written back to the main/shared memory. It would have been obvious to

one of ordinary skill in the memory art at the time the invention was made for the valid data to be provided to the requester by either the processor that modified the data or the main/shared memory because the processor that modified the data or the main/shared memory are the only sources for the valid data and official notice is taken thereof. Maintaining coherency in a multiprocessor system with a main/shared memory requires specific maintenance of the ownership of the data, otherwise, the data becomes corrupt and the data within this system is no longer reliable. Combining the requirement of only one processor having ownership rights to modify the data which sets forth situations in which only the processor with such ownership rights and possibly the main/shared memory also contain the modified data with the other limitations of the claims provides a well known method for maintaining data coherency within the system.

Regarding claims 2 and 10, Chang teach each of the processors communicates with the memory via a memory controller (col.4, lines 20-22) and each of the processors has a point-to-point link with the memory controller for issuing a request for a block of data to the memory controller (Fig.1 & Fig.2).

Regarding claims 3 and 11, Chang teach each point-to-point link includes two dedicated and unidirectional links (Fig.2, the lines indicating " to interconnect" and "from interconnect").

Regarding claims 4 and 12, Chang teach the point-to-point links are control links for sending and receiving requests for blocks of data (Fig. 2)

Regarding claims 5 and 13, Chang teach each of the processors has a control path point-to-point link for sending and receiving requests for blocks of data, and a data path point-to-point link for sending and receiving blocks of data (Fig. 2).

Regarding claim 6, Chang teach the processors and shared memory that have an invalid copy of the requested block of data drop the request without responding (col.11, lines 44-54)

Regarding claim 7, Chang teach tracking an identification of a processor that currently has a data block (Fig. 3, element 92); and in response to a cache miss in a requesting processor (Fig. 3), using the identification to specifically target a read request to the processor that currently has the requested data block (Fig. 3, col.7, lines 12-38).

Regarding claim 8, Chang teach maintaining a directory indicating the one or more processors that have a copy of a block of data (Fig.3 element 84); when the block of data is modified, using the directory to issue a write invalidation or write update only to the processors that have the copy of the block of data (col.7, lines 6-12).

Regarding claims 14,15 and 16, Chang teach a directory indicating which processors have a copy of a data block; wherein the processors are in communication with the directory to identify which other processors have a copy of the data block, and directing requests for the data block only to processors that have a copy of the data block (Fig. 3, col.6, lines 53 to col.7, lines 38).

Regarding claim 17, Chang teach the memory controller is in communication with a shared cache, separate from caches of the processors, for buffering most frequently accessed data block (col.7, lines 2-5).

Regarding claims 18, Chang teach each block has state information indicating which processor currently has a valid copy of a data block, and wherein the processors utilize the state information to specially address a processor having the valid copy in response to a cache miss in a requesting processor (Fig. 3, col.6, lines 47 to col.7, lines 2).

Regarding claim 20, Chang teach each of the processors and the shared memory is in communication with a control path interconnect, and each of the processors is in communication with the control path interconnect via a point-to point link for receiving and sending requests for blocks of data (Fig. 1 and Fig.2);

each of the processors having a corresponding request queue connecting the

point-to-point link of the processor to the control path interconnect (col.8, lines 34-40), and each of the processors having a corresponding snoop queue connecting the point-to-point link of the processor to the control path interconnect (col.4, lines 53-62);

the request queue in communication with a corresponding processor for buffering requests for blocks of data by the processor and issuing the requests to other processors via the control path interconnect (col.4, lines 49-53); and

the snoop queue in communication with a corresponding processor for buffering requests for blocks of data destined for the processor (col.4, lines 53-63).

Response to Amendment

5. Applicant's arguments filed 06/13/2002 have been fully considered but they are not persuasive.

6. In response to applicant's argument that Chang's reference teaches a pointer of an address of the data, but does not address the valid or invalid data. However, it is noted that the Chang's reference teaches that the validity of the contents of a TLB entry are indicated by a valid (v) bit that forms the first bit of a PTE (col.6, lines 60-62) and the valid bit of each PTE has to be checked (col.7, lines 26-27) before producing the physical address which used to utilize to access requested data (data in the cache can be either valid or invalid) in the cache (col.7, lines 33-38), the **requested data** in the cache is the valid data because only the valid data is provided to the requester by the processor or the main/shared memory in order to maintaining coherency in the

multiprocessor system with a main/shared memory requires specific maintenance of the ownership of the data, otherwise, the data becomes corrupt and the data within this system is no longer reliable. Importantly, the invalidation of the TLB entry or entries does not affect the processing of other marked and unmarked instructions (col.11, lines 17-21).

7. In response to applicant's request for art to backup the Examiner's official notice. The examiner is including as a reference U.S. Patent 6067626. "Only the processor or memory having the valid copy of the data block responds to the request" is taught as the second processor having valid data and transmit the valid data to the first processor in response to a signal from the first processor in this reference (claim 10, lines 7-9).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H. Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

September 5, 2002

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100